REMARKS

In response to the above-identified Office Action, Claims 15 and 17 are amended, no claims are cancelled and no claims are added. Accordingly, Claims 1-28 are pending and are rejected. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected under 35 U.S.C. §112

The Examiner rejects Claims 15 and 17 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicants regard as the invention.

Regarding Claim 15, Claim 15 has been amended to remove recitation to the claim features "the first gate" and "the third second gate" to resolve the antecedent basis problem identified by the Examiner. In addition, Claim 17 has been amended to remove the recitation to "the first gate" in line 2 of Claim 17 to resolve the antecedent basis issue pointed out by the Examiner.

Accordingly, Applicants respectfully submit that Claims 15 and 17, as amended, now provide antecedent basis for each of the recited features. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph, rejection of Claims 15 and 17.

II. Claim Objections

The Examiner objects to Claims 15 as being unclear. In response, Claim 15 is amended to recite the following claim features:

> wherein the non flow-through gate is a data flip-flop.

Applicants respectfully submit that Applicants' amendment to Claim 15 rectifies the claim objection identified by the Examiner. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the claim objection to Claim 15.

III. Double Patenting Rejection

The Examiner rejects Applicants' invention under the provisional obviousness-type double patenting rejection as not patentably distinct from the claimed inventions of U.S. Patent No. 6,748,513, although the conflicting claims are not identical. Applicants submit herewith a Terminal Disclaimer to overcome the double patenting rejection.

IV. Claim Rejections Under 35 U.S.C. §102

The Examiner rejects Claims 1, 11, 13, 18 and 26 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,061,293 issued to Miller ("Miller").

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Regarding Claim 1, Claim 1 recites the following claim feature, which is neither taught nor suggested by either Miller or the references of record:

> generating an enable signal in response to a digital address strobe signal and a digital address select signal to activate the enable signal prior to receipt of an address packet; and
>
> providing a flow-through path from an address pin to a chipset for a first component of the address packet in response to the enable signal, such that the first component of the address packet is provided to the chipset once the address packet appears on the address pin to expedite initiation of decoding of the address packet by the chipset. (Emphasis added.)

According to the Examiner, the above-recited features are taught by Miller with reference to col. 3, lines 9-67; col. 4, lines 1-27 and FIG. 2. (*See*, pg. 5, ¶3 of the Office Action mailed December 23, 2004.)

In contrast to the above-recited features of Claim 1, Miller teaches a source synchronous interface to convert the input signals to a protocol that is compatible with the timing requirements of a self-timed memory array. (*See*, col. 1, lines 53-56.)

As further described with reference to FIG. 2 of Miller, Miller teaches:

> Address bus 34 bits received from address bus pads 100-102 pass through two stages of latches. The first stage of latches, latch stage 80, includes the plurality of transparent latches 50-52 corresponding to each input buffer 40-42. The outputs of input buffers 40-42 are coupled to D-inputs of latches 50-52, respectively. Line 76 (ck# signal) is coupled to enable inputs of latches 50-52.
>
> In operation, latch 80 is controlled by the ck# signal only. (col. 4, lines 20–29.)

As further described by Miller:

> The two stages of latches, latch stages 80 and 82, work in conjunction to capture and hold data from address bus 34 for the duration of time required for tag memory array 70. (col. 4, lines 55-57.)

The operation of latch stages 80 and 82, is illustrated with reference to FIGS. 5-7 of Miller. As illustrated in FIGS. 5 and 6 of Miller, the enable input or address strobe for latch stage 82, as well as the pulse enable signal (CK 78) for latch stage 80 of Miller are not activated until after data appears in address bus 34. As described by Miller:

> The address data and address strobe are held until end operation 72 is received. (col. 5, lines 35-37.) (Emphasis added.)

Applicants respectfully submit that as specifically described by Miller, the two stages of latches (80 and 82) work in conjunction to capture and hold data from address bus 34 for the duration of time required for tag memory array to complete an access. (*See*, col. 4, lines 55-57.) Applicants respectfully submit that providing a flow through path within Miller, such that the information on address bus 34 is immediately provided to the memory array 70, as taught by Miller, would cause the address information to be overwritten and prohibit the capture and holding of data from address bus 34 for the duration of time required to tag memory array to complete an access. (*See*, col. 4, lines 55-57.)

Accordingly, Applicants respectfully submit that the enable signals for latch stage 80, as well as latch stage 82, as taught by Miller, are enabled following receipt of an address packet on address bus 34 and not prior to receipt of an address packet, as recited by Claim 1, to provide a flow through path of the first component of the address packet to the chipset once the address packet appears on the address pin. However, the case law is clear in establishing that an anticipatory reference must disclose each and every element of a claim to anticipate the claim and establish a *prima facie* case of anticipation. Id.

Hence, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation of Claim 1, since Miller does not disclose the above-recited features of activating an enable signal prior to receipt of an address packet on an address pin to provide a flow through path for first component of the address to a chipset once the address packet appears on the address pin. Id.

Consequently, Applicants respectfully submit that Claim 1 is patentable over Miller, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 1.

Regarding Claims 2-10, Claims 2-10, based on their dependency from Claim 1, are also patentable over Miller, as well as the references of record, for at least the reasons provided above. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 2-10.

Regarding Claim 11, Claim 11 recites the following claim features, which are neither taught nor suggested by either Miller or the references of record:

> a flow-through circuit to generate an enable signal in response to a digital address strobe signal and a digital address select signal to activate the enable signal prior to receipt of an address packet; and
>
> a flow-through gate having a digital address packet and the enable signal as inputs, the flow-through gate providing a first component of the digital address packet to a chipset in response to the enable signal once the digital address packet appears on the address pin, thereby providing a flow through path from the address pin to the chipset for the first component of the digital address packet to expedite initiation of decoding of the address packet by the chipset. (Emphasis added.)

For at least the reasons described above with reference to Claim 1, Applicants respectfully submit that the enable signal for latch stage 80 (CK 78) and the enable input for latch stage 82 are not activated until after receipt of an address packet and address bus 34. (*See*, FIGS. 5 and 6 of Miller.) Applicants respectfully submit that Miller fails to teach the above-recited features, since the teachings of Miller are directed to the use of two stages of latches, which work in combination to capture and hold data from an address bus for the duration of time required from a memory array to complete an access. (*See*, col. 4, lines 55-57 and col. 5, lines 3-13.) However, the case law in establishing that anticipation requires an anticipatory reference, which discloses each and every feature of the claim. Id.

Hence, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation of Claim 11, based on Miller, since Miller fails to disclose the generation of an enable signal prior to an address packet to enable a flow through path from an address pin to a chipset once the address packet appears on the address pin, as recited by Claim 11. Id. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 11.

Regarding Claims 12-19, Claims 12-19, based on their dependency from Claim 11, are also patentable over Miller, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 12-19.

V. Claim Rejections Under 35 U.S.C. §103

The Examiner rejects Claim 20 under 35 U.S.C. §103(a) as being unpatentable over Miller.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Pursuant to 35 U.S.C. §103(c), Miller is not an invalid §103(a) reference and therefore cannot be relied upon to preclude patentability of Claims 20-28 under 35 U.S.C. §103(a). Applicants respectfully submit that Miller only qualifies as prior art under one or more of subsections (e), (f) and (g) of 35 U.S.C. §102. Therefore, in accordance with §103(c), Miller is not a suitable §103(a) reference, since the subject matter described in Miller and the subject matter of all pending claims were, at the time the invention was made, commonly owned by the same entity or subject to an obligation of assignment of the same entity, Intel Corporation.

Accordingly, pursuant to 35 U.S.C. §103(c), Miller is an invalid §103(a) reference and therefore may not be used to preclude patentability of Claims 20-28 under 35 U.S.C. §103(a).

Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 20–28.

The Examiner rejects Claims 19 and 27 under 35 U.S.C. §103(a) as being unpatentable over the "Background of the Invention" section of Applicants' application as applied to Claims 1, 5, 6, 9, 13, 15 and 17, in view of U.S. Patent No. 6,385,710 issued to Goldman ("Goldman").

Regarding Claim 19, Claim 19, based on its dependency from Claim 11, recites the feature of a flow through circuit which generates an enable signal to activate prior to receipt of an address packet to provide a flow through path from an address pin for a first component of the address packet to a chipset. Applicants respectfully submit that the combination of the Background of the Invention, in addition with the features taught by Goldman, fail to teach or suggest the features of Claim 11, for at least the reasons indicated above.

Accordingly, Claim 11 is patentable over the combination of the Background of the Invention in view of Goldman. Consequently, Claim 19, based on its dependency from Claim 11, is also patentable over the combination of the Background of the Invention in view of Goldman. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 19.

Regarding Claim 27, Claim 27, based on its dependency from Claim 20, is also patentable over the combination of the Background of the Invention in view of Goldman, since combination fails to teach or suggest the flow through circuit and flow through grate, which activate an enable signal prior to receipt of an address packet to provide a flow through path from an address pin for a first component of the address packet to a chipset, to expedite decoding of the address packet, as recited by Claim 20.

Accordingly, Claim 20, as well as Claim 27, based on its dependency from Claim 20, are patentable over the combination of the Background of the Invention in view of Goldman. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 27.

CONCLUSION

Applicants have amended the claims to recite features that are not taught or suggested by the references. No new matter is introduced by the Applicants' claim amendments, which are supported in Applicants' specification and are necessary for placing the present application in condition for allowance.

In view of the foregoing, it is believed that all claims now pending, namely Claims 1-28 patentably define the present application over the prior art of record, and are therefore in condition for allowance; and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800, ext. 738.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: January 31, 2005

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 31, 2005

Marilyn Bass January 31, 2005